UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
KNOLL, CLIFFORD H

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/916,598	VENKITAKRISHNAN ET AL.
	Examiner	Art Unit
	Clifford H Knoll	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 October 2004</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 10/25/04. Currently

claims 1-20 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can

be found in a prior Office action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly
claiming the subject matter which the applicant regards as his invention.

1.   *Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being*

indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention.

In claims 1, 10, and 19, "that enable the processor units themselves" is unclear

because the correspondence among the processor units of the "cache coherent

snooping commands" and the instant processor units is not clear.

Claim Rejections - 35 USC § 102

2.   *Claims 1-4, 7, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by*

Arimilli (US 6587926).

Regarding claim 1, Arimilli discloses the processor units, cache units, embedded RAM (e.g., Figure 1), a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units themselves (col. 9, lines 39-45) to ensure cache coherency between the cache units for the processors and the embedded RAM unit (e.g., col. 2, lines 1-5).

Regarding claim 2, Arimilli also discloses an input output unit coupled to the bus to provide input and output transactions for the processor units (e.g., col. 5, lines 23-27).

Regarding claim 3, Arimilli also discloses the bus configured to provide split transactions for the processor units coupled to the bus (e.g., col. 5, lines 28-31).

Regarding claim 4, Arimilli also discloses the bus is configured to transfer an entire cache line for the cache units of the processor units (e.g., col. 7, lines 48-50).

Regarding claim 7, Arimilli also discloses support of a symmetric multiprocessing method for the plurality of processor units (e.g., col. 4, lines 49-55).

Regarding claim 9, Arimilli also discloses the processor units are configured to provide read data via the bus when the read data is stored within a respective cache unit (e.g., col. 7, lines 54-56).

Claim Rejections - 35 USC § 103

3.   *Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in*

view of standard practice of implementing buses, as further evidenced by Arimilli

(US 6571322, hereinafter Arimilli-2).

Regarding claim 5, Arimilli also discloses a system bus, but neglects to mention

the particular detail of bus width; however the Examiner takes Official Notice that the

256-bit wide system bus is a standard feature of cache coherent architectures. This is

further evidenced by Arimilli-2. Arimilli-2 discloses the bus is 256 bits wide (e.g., col. 9,

lines 7-8). It would be obvious to combine a standard bus width with Arimilli because

Arimilli discloses a particular cache coherency protocol that is useful with standard

system buses. Therefore it would have been obvious to a person of ordinary skill in the

art at the time the invention was made to combine Arimilli with the standard system bus

width of 256 bits.

4.   *Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in*

view of Arimilli-2.

Regarding claim 5, Arimilli also discloses a system bus, but neglects to mention

the particular detail of bus width; however this feature is disclosed by Arimilli-2. Arimilli-

2 discloses the bus is 256 bits wide (e.g., col. 9, lines 7-8). A person of ordinary skill in

the art would be motivated to combine Arimilli-2 with Arimilli because Arimilli-2 teaches

the improvement of a cache coherent system, such as Arimilli, by accommodating the

standard system bus width of 256 bits as a sector that does not need to be invalidated

(e.g., col. 5, lines 35-38). Therefore it would be obvious to one of ordinary skill in the art

to combine Arimilli-2 with Arimilli at the time the invention was made to obtain the

claimed invention.

5.   *Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in*

view of standard practice of memory implementation, as further evidenced by Miller

(6560682).

Regarding claim 6, Arimilli discloses an embedded RAM core, but fails to

disclose the detail of using DRAM to implement memory; however the examiner takes

Official Notice that the use of a DRAM core is standard embodiment of a RAM memory.

This is further evidenced by Miller. Miller discloses the embedded DRAM core (e.g.,

col. 5, lines 7-10). It would be obvious to combine the DRAM implementation of

memory with Arimilli because the embedded DRAM core is a standard means to

implement a RAM unit. Therefore it would be obvious to one of ordinary skill in the art

to combine a standard memory embodiment with the disclosure of Arimilli.

6.   *Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in*

view of standard embodiment of a processor, as further evidenced by Bitar (US

6418460).

Regarding claim 8, Arimilli neglects to disclose implementational details of a

particular processor core; however the Examiner takes Official Notice that MIPS

architecture is a standard processor and is well-known for its implementation in symmetric multiprocessing systems, such as in the system of Arimilli. This is further evidenced by Bitar. Bitar discloses the multi-processor units are compatible with a version of a MIPS processor core (e.g., Figure 2B, col. 13, line 39; and col. 17, lines 13-14 in the context of multiprocessor systems). It would be obvious to combine Arimilli with the standard MIPS architecture, because the use of MIPS architecture is widely known in the implementation of symmetric multiprocessing systems such as the system of Arimilli. Therefore at the time the invention was made, it would be obvious to a person of ordinary skill in the art to combine the MIPS architecture, as evidenced by Bitar, with Arimilli to obtain the claimed invention.

7.   *Claims 10-13, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of the standard practice of integrating circuits, as further evidenced by Sherburne (2002/0184546).*

Regarding claim 10, Arimilli discloses a power supply; a plurality of processor units; a plurality of cache units, one of the cache units provided for each one of the processor units; an embedded RAM unit for storing instructions and data for the processor units (e.g., Figure 1); a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units themselves (col. 9, lines 39-45) to ensure cache coherency between the cache units for the processor units and the embedded RAM unit (e.g., col. 2, lines 1-5). Arimilli does not expressly mention a particular embodiment of

an integrated circuit die; however the Examiner takes Official Notice that it is manifestly

obvious to integrate multi-processing devices for the well-known and well-noted

advantages of portability, power consumption, and so forth. This is further evidenced by

Sherburne. Sherburne discloses the well-known practice of using highly integrated

devices to obtain the advantages of decreased size and weight (e.g., paragraph [0002]).

It would be obvious to combine Arimilli with the well-known practice of integration

because the practice is standard and the advantages for doing so are well established

in areas such as those evidenced by Sherburne, which included multiprocessing

systems with cache and embedded memory. Therefore it would be obvious to one of

ordinary skill in the art to combine Arimilli with the standard practice of integration.

Regarding claim 11, Arimilli also discloses an input output unit coupled to the bus

to provide input and output transactions for the processor units (e.g., col. 5, lines 23-27).

Regarding claim 12, Arimilli also discloses the bus configured to provide split

transactions for the processor units coupled to the bus (e.g., col. 5, lines 28-31).

Regarding claim 13, Arimilli also discloses the bus is configured to transfer an

entire cache line for the cache units of the processor units (e.g., col. 7, lines 48-50).

Regarding claim 16, Arimilli also discloses support of a symmetric

multiprocessing method for the plurality of processor units (e.g., col. 4, lines 49-55).

Regarding claim 18, Arimilli also discloses the processor units are configured to

provide read data via the bus when the read data is stored within a respective cache

unit (e.g., col. 7, lines 54-56).

8.   *Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli*

         and the standard practice of integration, as applied in claim 10 above, further in view

         of Arimilli-2.

         Regarding claim 14, Arimilli also discloses a system bus, but neglects to mention

the particular detail of bus width; however this feature is disclosed by Arimilli-2. Arimilli-

2 discloses the bus is 256 bits wide (e.g., col. 9, lines 7-8). A person of ordinary skill in

the art would be motivated to combine Arimilli-2 with Arimilli because Arimilli-2 teaches

the improvement of a cache coherent system, such as Arimilli, by accommodating the

standard system bus width of 256 bits as a sector that does not need to be invalidated

(e.g., col. 5, lines 35-38). Therefore it would be obvious to one of ordinary skill in the art

to combine Arimilli-2 with Arimilli and the well-known practice of integration at the time

the invention was made to obtain the claimed invention.

9.   *Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli*

         and the standard practice of integration, as applied in claim 10 above, further in view

         of the standard practice of memory implementation, as further evidenced by Miller.

         Regarding claim 15, Arimilli fails to disclose the detail of using DRAM to

implement memory; however the examiner takes Official Notice that the use of a DRAM

core is standard embodiment of a RAM memory. This is further evidenced by Miller.

Miller discloses the embedded DRAM core (e.g., col. 5, lines 7-10). It would be obvious

to combine standard implementation practice with Arimilli because the DRAM is a

standard means to implement an embedded RAM core. Therefore it would be obvious

to one of ordinary skill in the art to combine a standard memory embodiment with the

disclosure of Arimilli and the well-known practice of integration.

10.   *Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli*

       and the standard practice of integration, as applied in claim 10 above, further in view

       of a standard processor embodiment, as evidenced by Miller.

       Regarding claim 17, Arimilli neglects to disclose implementational details of a

particular processor core; however the Examiner takes Official Notice that MIPS

architecture is a standard processor for symmetric multiprocessing, such as in the

system of Arimilli. This is further evidenced by Bitar. Bitar discloses the processor units

are compatible with a version of a MIPS processor core (e.g., Figure 2B, col. 13, line 39;

and col. 17, lines 13-14 in the context of multiprocessor systems). It would be obvious

to combine Arimilli with the standard MIPS architecture, because the use of MIPS

architecture is standard in the implementation of symmetric multiprocessing systems

such as the system of Arimilli. Therefore at the time the invention was made, it would

be obvious to a person of ordinary skill in the art to combine the MIPS architecture, a

standard embodiment as evidenced by Bitar, with Arimilli and the standard practice of

integration to obtain the claimed invention.

11.   *Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable*

       over Arimilli, in view of standard practice of integration and memory implementation,

       as evidenced by Sherburne, and further in view of Arimilli-2.

Regarding claim 19, Arimilli discloses and a power supply, a plurality of processor units; a plurality of cache units, one of the cache units provided for each one of the processor units; an embedded RAM core unit for storing instructions and data for the processor units (e.g., Figure 1); a cache coherent bus coupled to the processor units and the embedded RAM core unit, the bus configured to provide cache coherent snooping commands from the processor units themselves (col. 9, lines 39-45) to ensure cache coherency between the cache units for the processor units and the embedded RAM core unit (e.g., col. 2, lines 1-5). Arimilli does not expressly mention a particular embodiment of an integrated circuit die and said invention occurring in a portable hand-held device; however the Examiner takes Official Notice that it is manifestly obvious to integrate multi-processing devices for the well-known and well-noted advantages of portability, power consumption, and so forth. Likewise, the Examiner also takes Official Notice that the use of DRAM as a memory implementation is standard practice. This also is further evidenced by Sherburne. Sherburne discloses the well-known practice of using highly integrated devices rendering the advantages of decreased size and weight (e.g., paragraph [0002]) as well as the manifest advantages of portability in a use such as handheld device (e.g., paragraph [0002]) and also the use of DRAM to implement memory (e.g., Figure 1). It would be obvious to combine Arimilli with the well-known practice of integration because the practice is standard and the advantages for doing so are well established in areas such as those evidenced by Sherburne, which include multiprocessing systems with cache and embedded memory. Likewise the use of DRAM to implement memory as, evidenced by Sherburne, is standard practice.

Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli with the standard practice of integration.

Arimilli also discloses a system bus, but neglects to mention the particular detail of bus width; however this feature is disclosed by Arimilli-2. Arimilli-2 discloses the bus is 256 bits wide (e.g., col. 9, lines 7-8). A person of ordinary skill in the art would be motivated to combine Arimilli-2 with Arimilli because Arimilli-2 teaches the improvement of a cache coherent system, such as Arimilli, by accommodating the standard system bus width of 256 bits as a sector that does not necessarily need to be invalidated (e.g., col. 5, lines 35-38). Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli-2 with Arimilli and the well-known practice of integration at the time the invention was made to obtain the claimed invention.

Regarding claim 20, Arimilli also discloses the bus configured to provide split transactions for the processor units coupled to the bus (e.g., col. 5, lines 28-31).

Response to Arguments

Applicant's arguments filed 10/25/04 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that in Arimilli, "nothing in the referenced passage indicates that: (1) a processor, (2) maintain cache coherency, (3) between a processor cache unit and a RAM unit as is recited in Claim 1" (p. 7); however, Arimilli teaches just this. For example, processors, cache, and a RAM unit ("System Memory")

are clearly seen in Figure 1, while maintaining cache coherency is the chief concern of aspects of the disclosure depicted in Figures 5 and 6 ("Coherency Update Needed?").

Applicant further argues that "nowhere in the Arimilli et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency" (p. 7); however to the extent that the recitation can be clearly interpreted, as Arimilli discloses, "[i]f, as illustrated at steps 606 and 608, the snooping device is a potential third party transactor, the scarf tag field designated for the memory level at which the snooper resides is compared with the snoopers device identification tag. If a match is found at step 610, the process continues at step 618 with the snoop device writing the target data into its memory" (col. 9, lines 39-45). The "third party transactor" functions by itself as the "snoop device" which is clearly an aspect of the processor, itself, concerned with maintaining coherency.

Regarding claims 5-6 and 8, Applicant argues that Arimilli does not "show or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to 'provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit'" (pp. 9-10); however, as recited, Arimilli teaches this, as treated supra regarding claim 1.

Regarding claims 10, 14-15, and 17, Applicant argues that Arimilli does not "show or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to 'provide cache coherent snooping commands from the processor

units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit'" (pp. 11-14); however, Sherburne is not relied upon for this disclosure. As recited, Arimilli teaches this, as treated supra regarding similar recitation in claim 1.

Regarding claim 19, Applicant argues that Arimilli does not "show or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to 'provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit'" (p. 15); however, as recited, Arimilli teaches this, as treated supra regarding similar recitation in claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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PRIMARY EXAMINER